OPA2604 Dual FET-Input, Low-Distortion Operational Amplifier

1 Features

- Low Distortion: 0.0003% at 1 kHz
- Low Noise: 10 nV/√Hz
- High Slew Rate: 25 V/µs
- Wide Gain-Bandwidth: 20 MHz
- Unity-Gain Stable
- Wide Supply Range: V_S = ±4.5 to ±24 V
- Drives 600-Ω Loads

2 Applications

- Professional Audio Equipment
- PCM DAC I/V Converters
- Spectral Analysis Equipment
- Active Filters
- Transducer Amplifiers
- Data Acquisition

3 Description

The OPA2604 is a dual, FET-input operational amplifier designed for enhanced AC performance. Low distortion, low noise, and wide bandwidth provide superior performance in high quality audio and other applications requiring dynamic performance.

New circuit techniques and special laser-trimming of dynamic circuit performance yield low harmonic distortion. The result is an operational amplifier with exceptional sound quality. The low-noise FET input of the OPA2604 provides wide dynamic range, even with high source impedance. Offset voltage is laser-trimmed to minimize the need for interstage coupling capacitors.

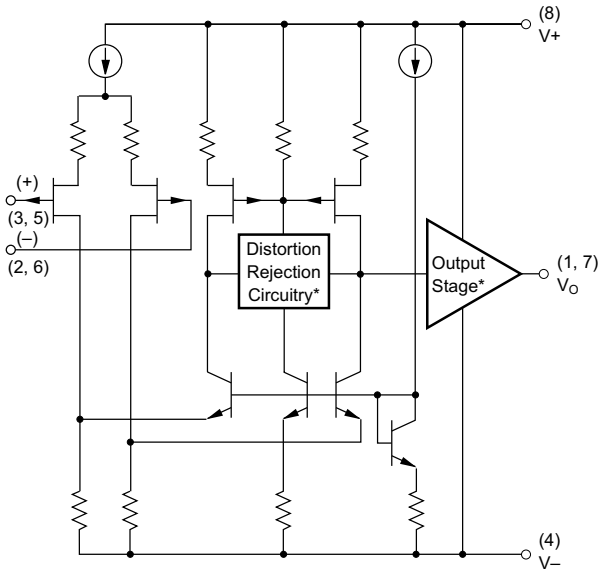
The OPA2604 is available in 8-pin plastic mini-DIP and 8-Pin SOIC surface-mount packages, specified for the –25°C to 85°C temperature range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA2604	SOIC (8)	3.91 mm × 4.90 mm
	PDIP (8)	6.35 mm × 9.81 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



* Patents Granted:
#5053718, 5019789

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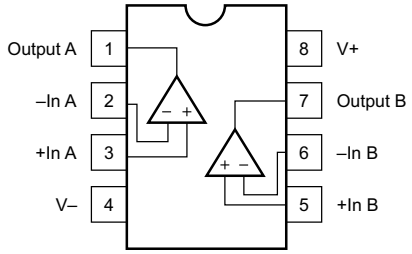
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2000) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

5 Pin Configuration and Functions

P and D Packages
8-Pin PDIP and SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	Output A	O	Output channel A
2	–In A	I	Inverting input channel A
3	+In A	I	Noninverting input channel A
4	V–	I	Negative power supply
5	+In B	I	Noninverting input channel B
6	–In B	I	Inverting input channel B
7	Output B	O	Output channel B
8	V+	I	Positive power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
	Power supply voltage		±25	V
	Input voltage	(V–)–1	(V+)+1	V
	Output short-circuit to ground	Continuous		
	Operating temperature	–40	100	°C
	Junction temperature		150	°C
	Lead temperature (soldering, 10 s) AP		300	°C
	Lead temperature (soldering, 3 s) AU		260	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
OPA2604 in SOIC Package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	
OPA2604 in PDIP Package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V+, V–	Power supply voltage	±4.5	±15	±24	V
	Operating temperature	–40		100	°C

6.4 Thermal Information

THERMAL METRIC (1)		OPA2604		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.9	46.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.3	35	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	24	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.7	12.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.9	23.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input offset voltage				±1	±5	mV
Average drift				±8		µV/°C
Power supply rejection		V_S = ±5 to ±24 V	70	80		dB
INPUT BIAS CURRENT(1)						
Input bias current		V_{CM} = 0 V		100		pA
Input offset current		V_{CM} = 0 V		±4		pA
INPUT VOLTAGE NOISE						
Noise density	f = 10 Hz			25		nV/√Hz
	f = 100 Hz			15		
	f = 1 kHz			11		
	f = 10 kHz			10		
Voltage noise, BW = 20 Hz to 20 kHz				1.5		µVp-p
INPUT BIAS NOISE						
Current noise density, f = 0.1 Hz to 20 kHz				6		fA/√Hz
INPUT VOLTAGE RANGE						
Common-mode input range			±12	±13		V
Common-mode rejection		V_{CM} = ±12 V	80	100		dB
INPUT IMPEDANCE						
Differential				10^{12} || 8		Ω || pF
Common-mode				10^{12} || 10		Ω || pF
OPEN-LOOP GAIN						
Open-loop voltage gain		V_O = ±10 V, R_L = 1 kΩ	80	100		dB
FREQUENCY RESPONSE						
Gain-bandwidth product		G = 100		20		MHz
Slew rate		20 Vp-p, R_L = 1 kΩ	15	25		V/µs
Settling time	0.01%	G = –1, 10-V Step		1.5		µs
	0.1%			1		
Total harmonic distortion + noise (THD+N)		G = 1, f = 1 kHz V_O = 3.5 Vrms, R_L = 1 kΩ		0.0003%		
Channel separation		f = 1 kHz, R_L = 1 kΩ		142		dB
OUTPUT						
Voltage output		R_L = 600 Ω	±11	±12		V
Current output		V_O = ±12 V		±35		mA
Short circuit current				±40		mA
Output resistance, open-loop				25		Ω
POWER SUPPLY						
Specified operating voltage				±15		V
Operating voltage range			±4.5		±24	V
Current, total both amplifiers		I_O = 0		±10.5	±12	mA
TEMPERATURE RANGE						
Specification			–25		85	°C

(1) Typical performance, measured fully warmed-up.

6.6 Typical Characteristics

at T_A = 25°C, V_S = ±15 V (unless otherwise noted)

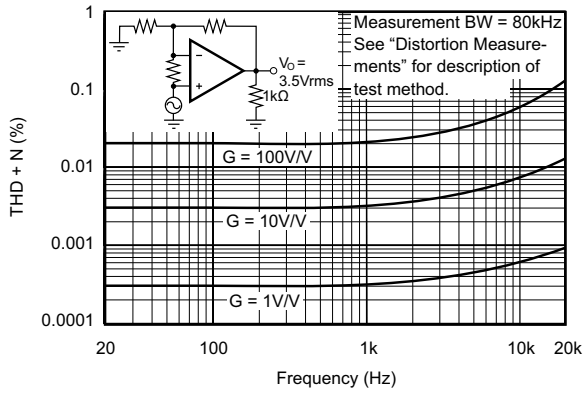


Figure 1. Total Harmonic Distortion + Noise vs Frequency

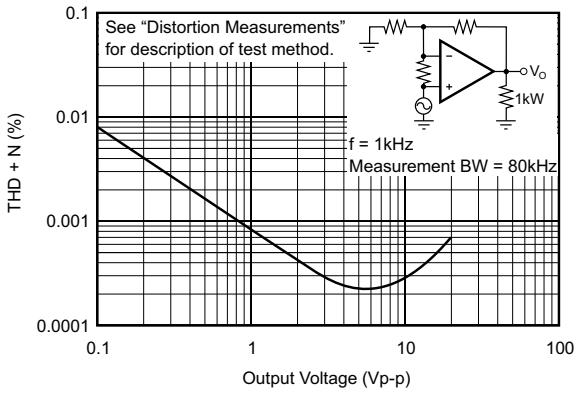


Figure 2. Total Harmonic Distortion + Noise vs Output Voltage

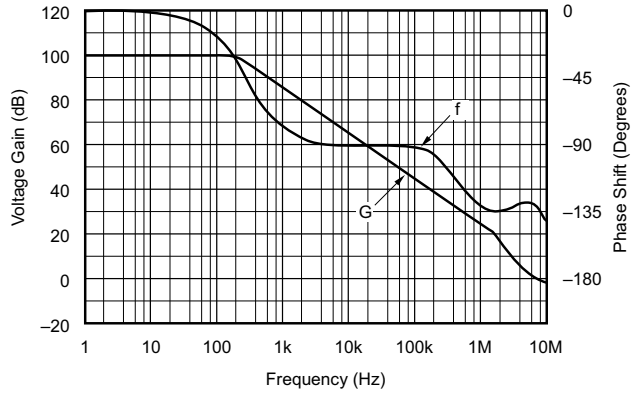


Figure 3. Open-Loop Gain and Phase vs Frequency

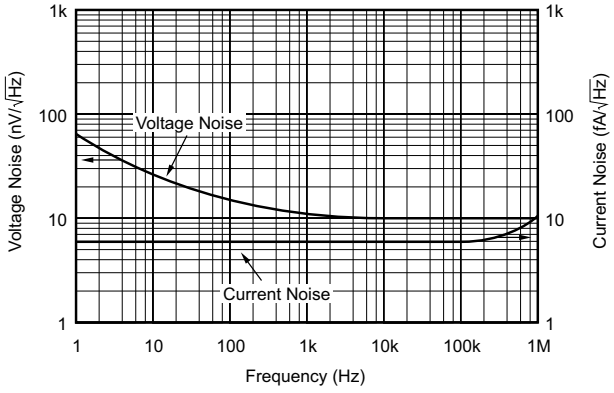


Figure 4. Input Voltage and Current Noise Spectral Density vs Frequency

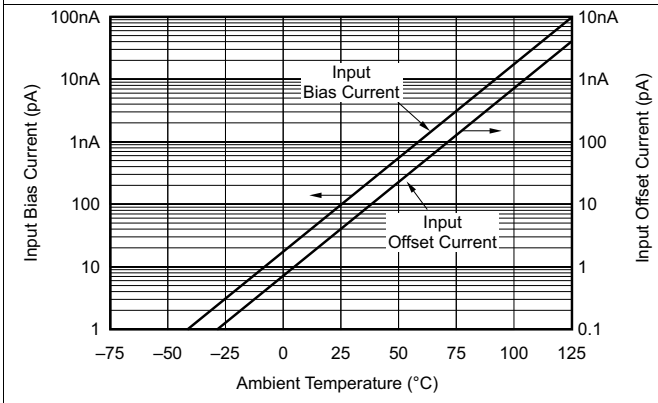


Figure 5. Input Bias and Input Offset Current vs Temperature

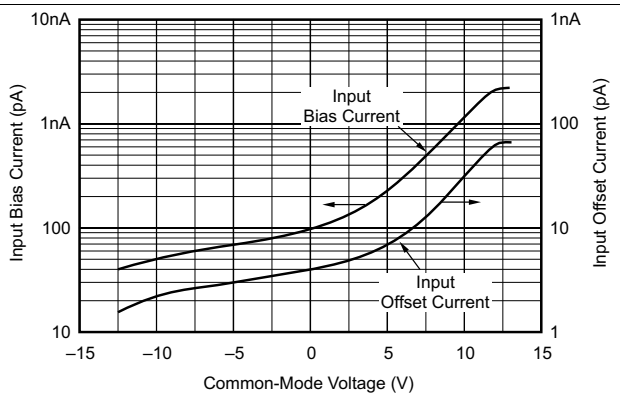


Figure 6. Input Bias and Input Offset Current vs Input Common-Mode Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V (unless otherwise noted)

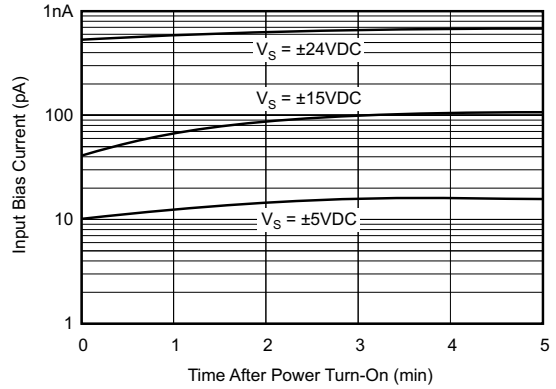


Figure 7. Input Bias Current vs Time from Power Turnon

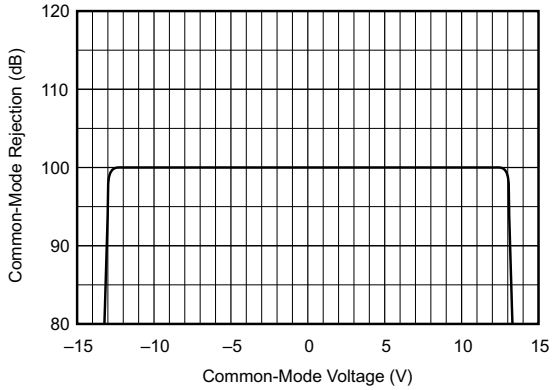


Figure 8. Common-Mode Rejection vs Common-Mode Voltage

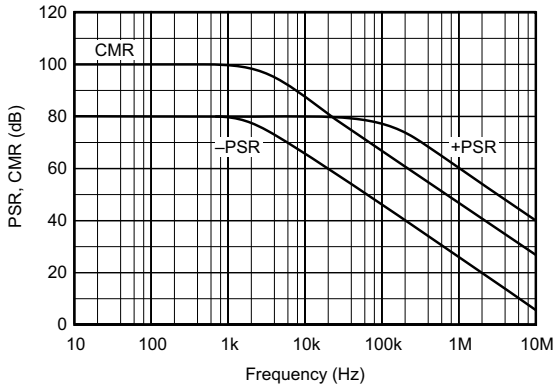


Figure 9. Power Supply and Common-Mode Rejection vs Frequency

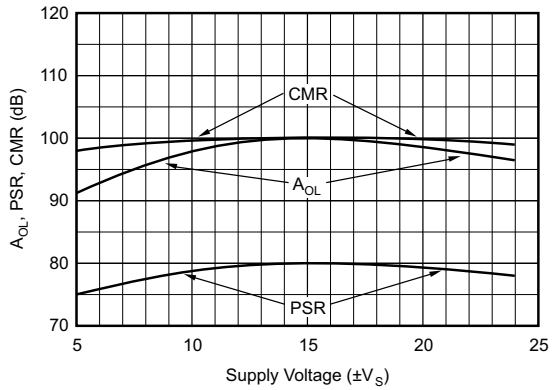


Figure 10. A_{OL}, PSR, and CMR vs Supply Voltage

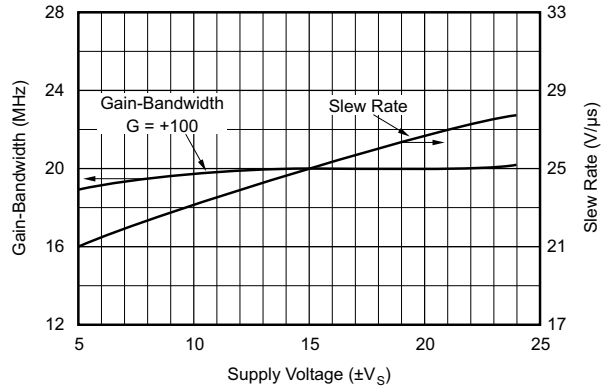


Figure 11. Gain-Bandwidth and Slew Rate vs Supply Voltage

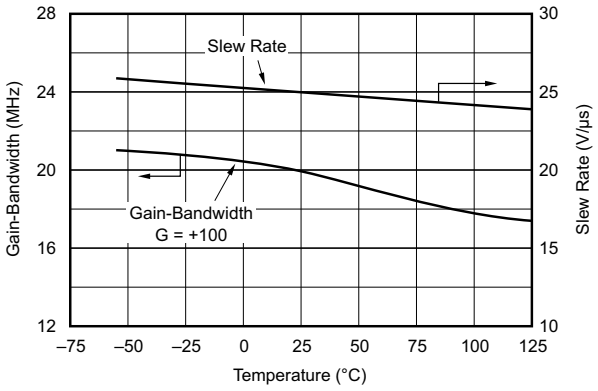


Figure 12. Gain-Bandwidth and Slew Rate vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V (unless otherwise noted)

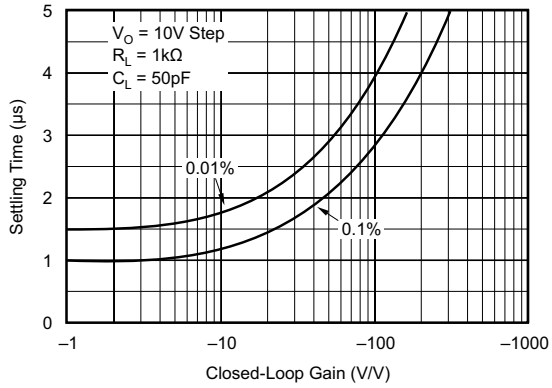


Figure 13. Settling Time vs Closed-Loop Gain

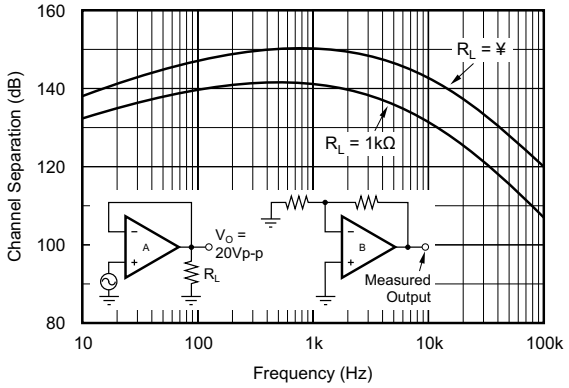


Figure 14. Channel Separation vs Frequency

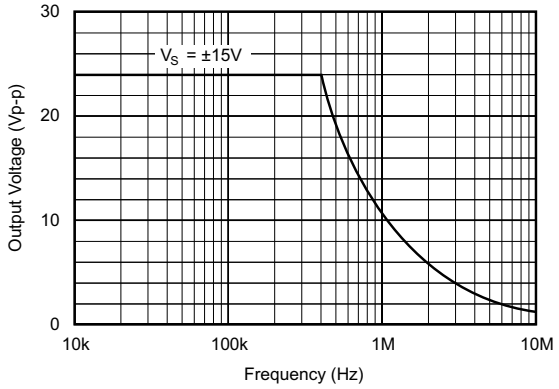


Figure 15. Maximum Output Voltage Swing vs Frequency

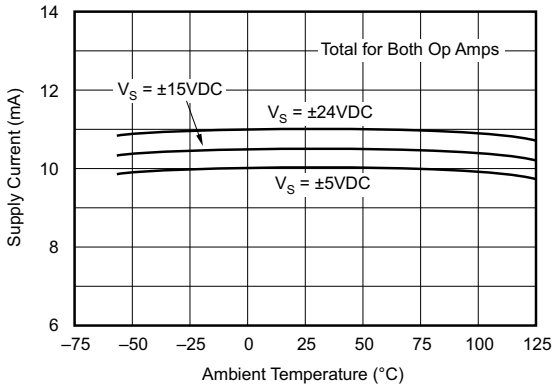


Figure 16. Supply Current vs Temperature

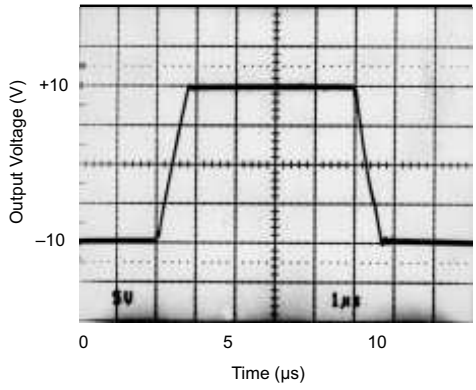


Figure 17. Large-Signal Transient Response

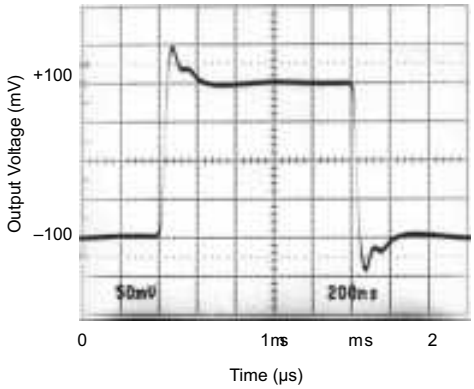


Figure 18. Small-Signal Transient Response

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V (unless otherwise noted)

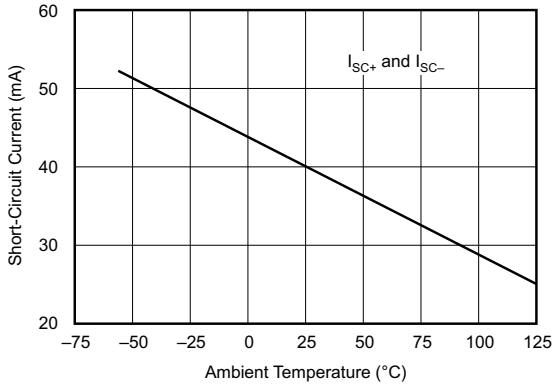


Figure 19. Short Circuit Current vs Temperature

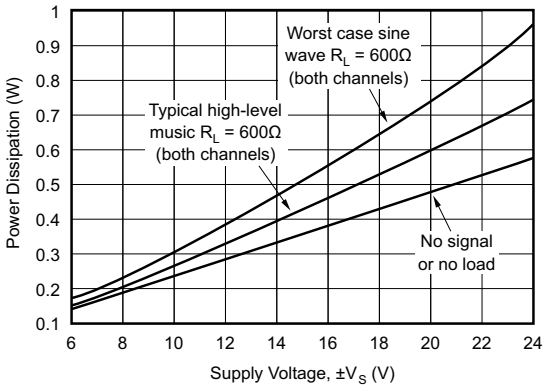


Figure 20. Power Dissipation vs Supply Voltage

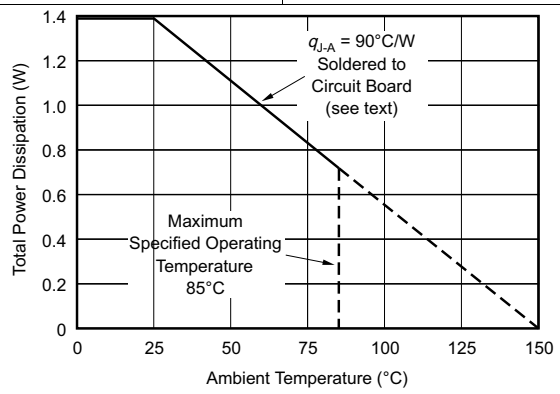


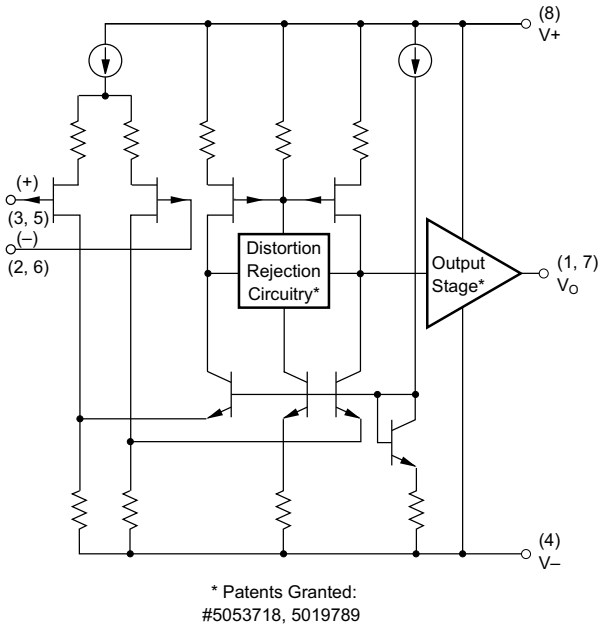
Figure 21. Maximum Power Dissipation vs Temperature

7 Detailed Description

7.1 Overview

The OPA2604 is a dual, FET-input operational amplifier designed for enhanced AC performance. Low distortion, low noise, and wide bandwidth provide superior performance in high quality audio and other applications requiring dynamic performance.

7.2 Functional Block Diagram



* Patents Granted:
#5053718, 5019789

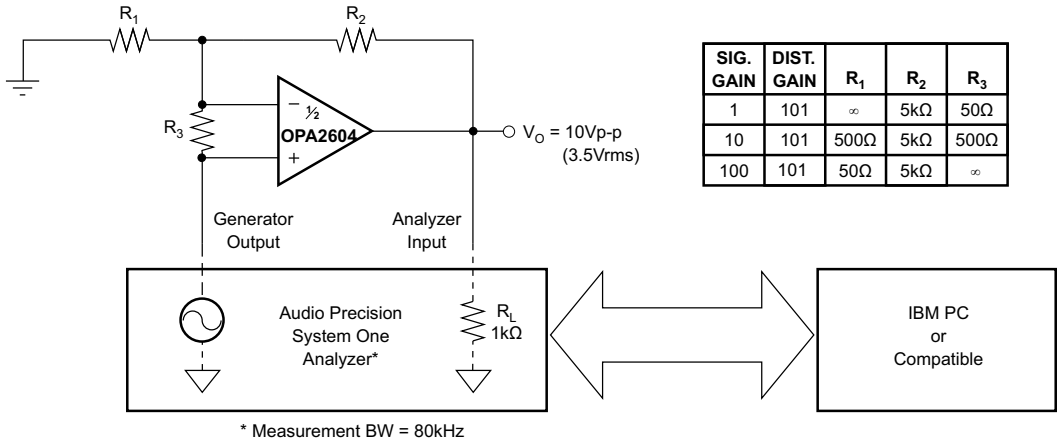
7.3 Feature Description

7.3.1 Distortion

The distortion produced by the OPA2604 is below the measurement limit of virtually all commercially available equipment. A special test circuit, however, can extend the measurement capabilities.

Op amp distortion can be considered an internal error source, which can be referred to the input. Figure 22 shows a circuit that causes the op amp distortion to be 101 times more than normally produced. The addition of R_3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101. This extends the measurement limit, including the effects of the signal-source purity, by a factor of 101. The input signal and load applied to the op amp are the same as with conventional feedback without R_3.

Feature Description (continued)



SIG. GAIN	DIST. GAIN	R_1	R_2	R_3
1	101	∞	5kΩ	50Ω
10	101	500Ω	5kΩ	500Ω
100	101	50Ω	5kΩ	∞

Figure 22. Distortion Test Circuit

Validity of this technique can be verified by duplicating measurements at high gain or high frequency, where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with the Audio Precision System One, which simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

7.3.2 Capacitive Loads

The dynamic characteristics of the OPA2604 are optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and capacitive load decreases the phase margin and may lead to gain-peaking or oscillations. Load capacitance reacts with the open-loop output resistance of the op amp to form an additional pole in the feedback loop. Figure 23 shows various circuits which preserve phase margin with capacitive load. Request Application Bulletin AB-028 for details of analysis techniques and applications circuits.

Feature Description (continued)

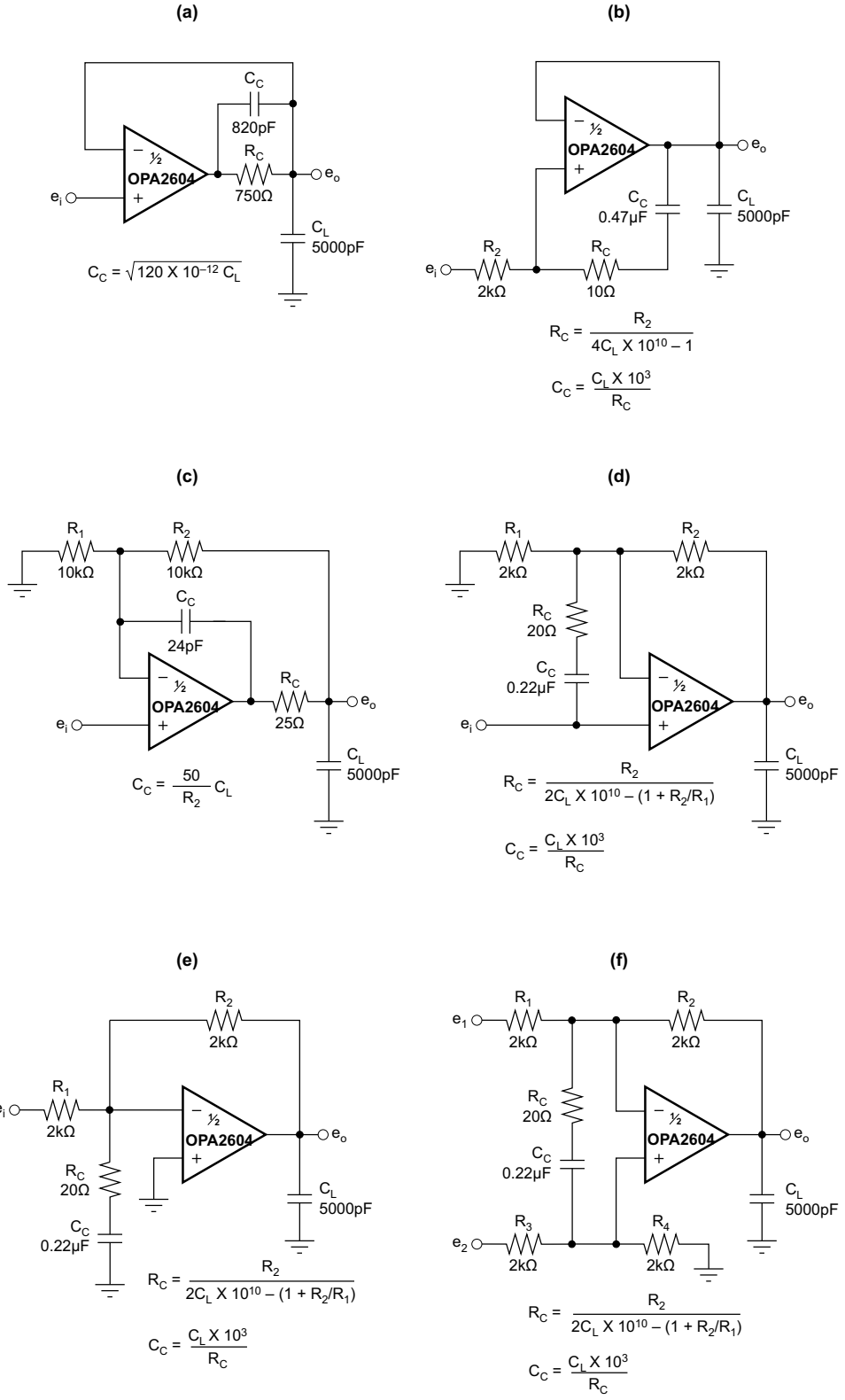


Figure 23. Driving Large Capacitive Loads

Feature Description (continued)

For the unity-gain buffer, (a) in Figure 23, stability is preserved by adding a phase-lead network, R_C and C_C. Voltage drop across R_C reduces output voltage swing with heavy loads. An alternate circuit, (b), does not limit the output with low load impedance, and provides a small amount of positive feedback to reduce the net feedback factor. Input impedance of this circuit falls at high frequency, as op amp gain rolloff reduces the bootstrap action on the compensation network.

In Figure 23, (c) and (d) show compensation techniques for noninverting amplifiers. Like the follower circuits, the circuit in (d) eliminates voltage drop due to load current, but at the penalty of somewhat reduced input impedance at high frequency.

In Figure 23, (e) and (f) show input lead compensation networks for inverting and difference amplifier configurations.

7.3.3 Noise Performance

Op amp noise is described by two parameters: noise voltage and noise current. The voltage noise determines the noise performance with low source impedance. Low noise bipolar-input op amps such as the OPA27 and OPA37 provide low voltage noise. However, if source impedance is greater than a few thousand Ωs, the current noise of bipolar-input op amps react with the source impedance and dominate. At a few thousand Ωs source impedance and above, the OPA2604 generally provides lower noise.

7.4 Device Functional Modes

The OPA2604 has a single functional mode and is operational when the power-supply voltage is greater than ±4.5 V. The maximum power supply voltage for the OPA2604 ±24 V.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Low pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPA2604 is ideally suited to construct high-speed, high-precision active filters. Figure 24 illustrates a second order low pass filter commonly encountered in signal processing applications.

8.2 Typical Applications

8.2.1 25-kHz Low Pass Filter

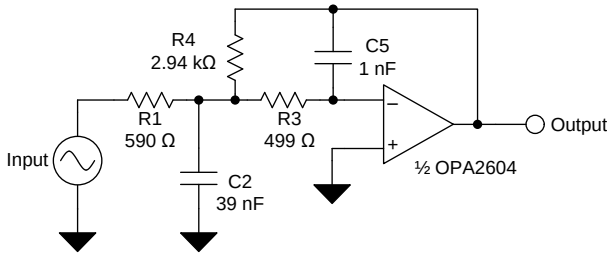


Figure 24. 25 kHz Low Pass Filter Schematic

8.2.1.1 Design Requirements

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain).
- Low pass cutoff frequency = 25 kHz.
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband.

8.2.1.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Equation 1. Use Equation 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit the gain at DC and the low pass cutoff frequency can be calculated using Equation 2.

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (2)$$

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners. Available as a web based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multi-stage active filter solutions within minutes.

Typical Applications (continued)

8.2.1.3 Application Curve

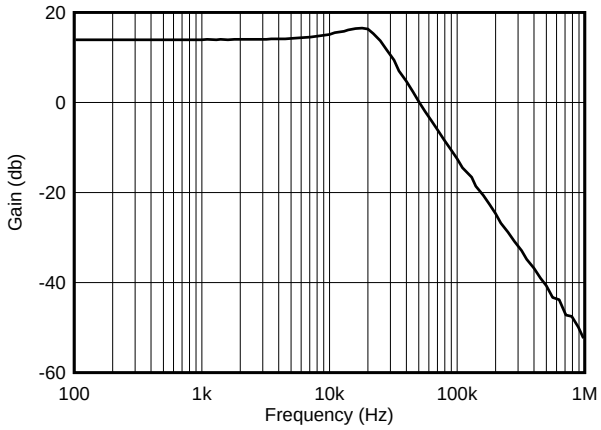


Figure 25. 25-kHz Low Pass Filter Response

8.2.2 Three-Pole Generalized-Immittance Converter (GIC) Low-Pass Filter

In any digitizing system, anti-aliasing and anti-imaging filters are used to prevent the signal frequencies from folding back around the sample frequency and causing false (or alias) signals from appearing in the signal we are attempting to digitize. Very often, these filters must be very complex, high order analog filters to do their job effectively.

The filter characteristic most desirable for sensitive DSP type applications is linear-phase. The linear-phase filter is sometimes called a Bessel (or Thomson) filter. The linear-phase filter has constant group delay. This means that the phase of the filter changes linearly with frequency, or that the group delay is constant. These filters maintain phase information for sensitive DSP applications such as correlation, and preserve transient response. These characteristics are critical in audio applications as well, because they affect sound quality greatly. Illustrated in Figure 26 is a third-order low pass filter with 40-kHz cutoff frequency designed for audio applications.

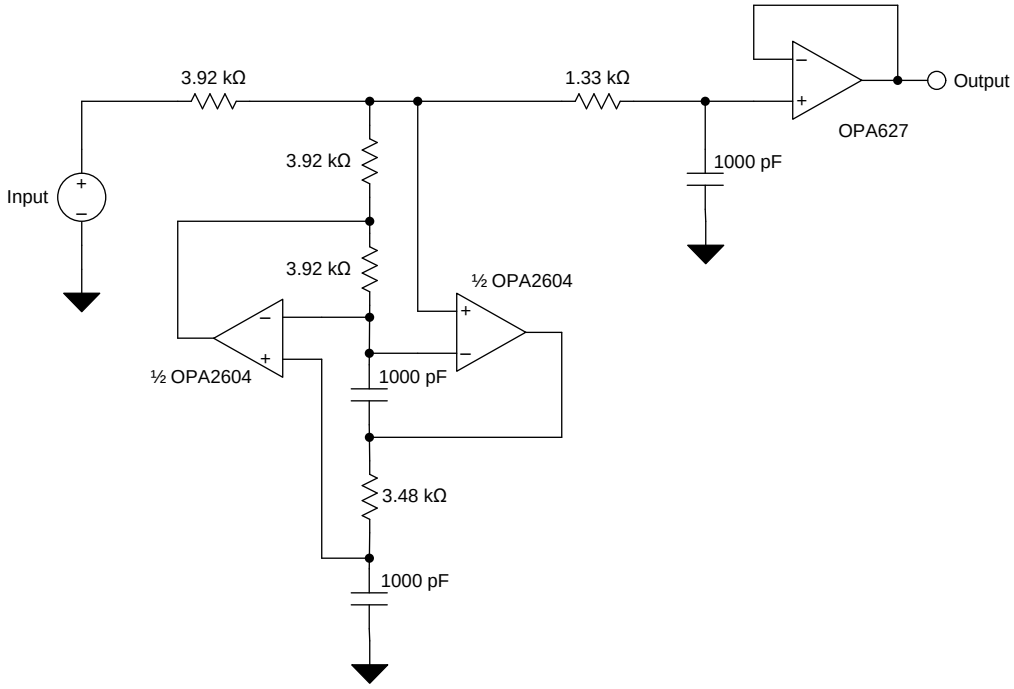


Figure 26. Three-Pole Generalized-Immittance Converter (GIC) Low-Pass Filter

Typical Applications (continued)

8.2.2.1 Design Requirements

The filter shown in Figure 26 is intended to meet the following design requirements:

- Third-order low pass filter response
- 40-kHz cutoff frequency
- Linear phase
- Constant group delay

8.2.3 DAC I/V Amplifier and Low-Pass Filter

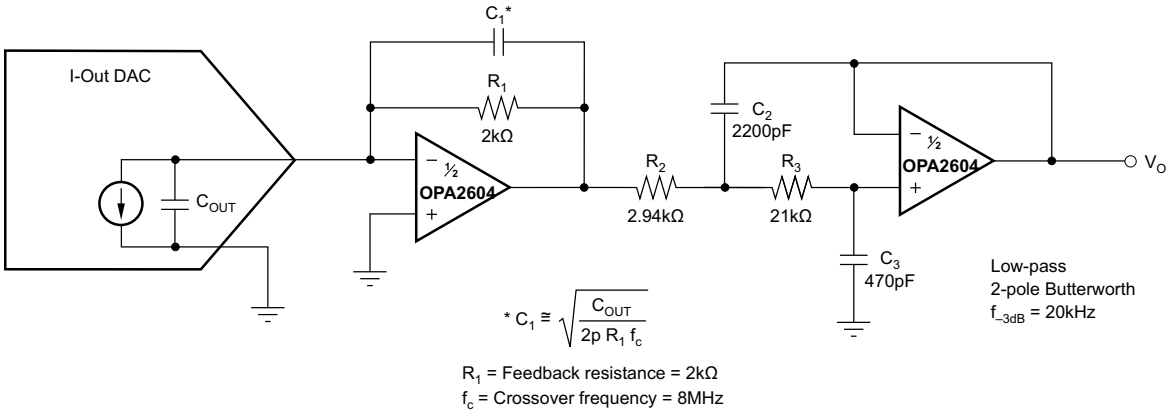


Figure 27. DAC I/V Amplifier and Low-Pass Filter

8.2.3.1 Design Requirements

The current to voltage converter shown in Figure 27 is intended to meet the following design requirements:

- Second-order low pass filter response
- 8-MHz cutoff frequency
- Butterworth response
- 2-kΩ transimpedance

Typical Applications (continued)

8.2.4 Differential Amplifier with Low-Pass Filter

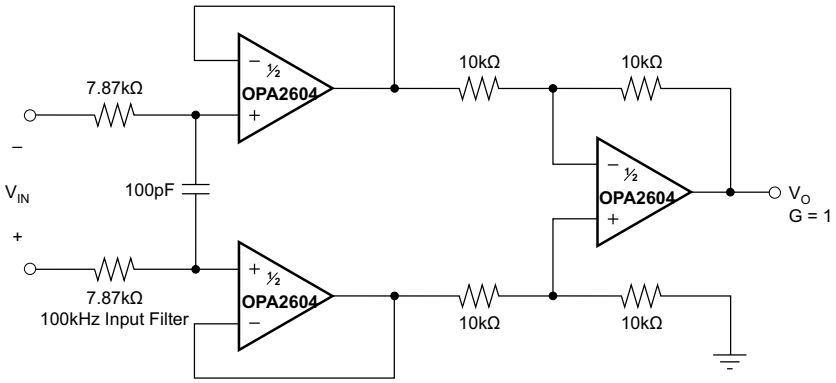


Figure 28. Differential Amplifier with Low-Pass Filter

8.2.4.1 Design Requirements

The differential amplifier shown in Figure 28 is intended to meet the following design requirements:

- First-order low pass filter response
- 100-kHz cutoff frequency
- Differential gain = 1 V/V

8.2.5 High Impedance Amplifier

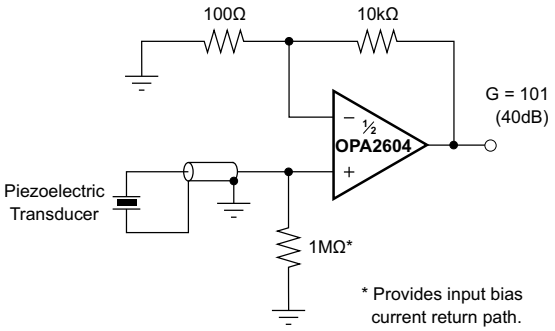


Figure 29. High Impedance Amplifier

8.2.5.1 Design Requirements

The high impedance amplifier shown in Figure 29 is intended to meet the following design requirements:

- 40-db gain
- Input leakage current less than 100 pA

Typical Applications (continued)

8.2.6 Digital Audio DAC I-V Amplifier

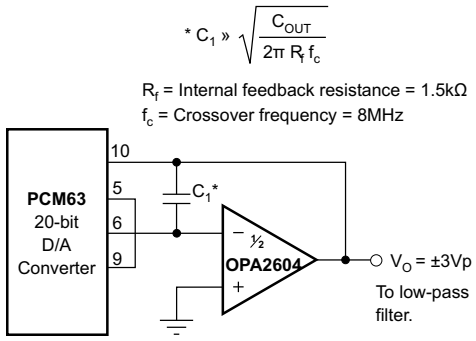


Figure 30. Digital Audio DAC I-V Amplifier

8.2.6.1 Design Requirements

The digital audio current to voltage converter shown in Figure 30 is intended to meet the following design requirements:

- First-order low pass filter response
- 8-MHz cutoff frequency
- 1.5-kΩ transimpedance

8.2.7 Using the Dual OPA2604 Op Amp to Double the Output Current to a Load

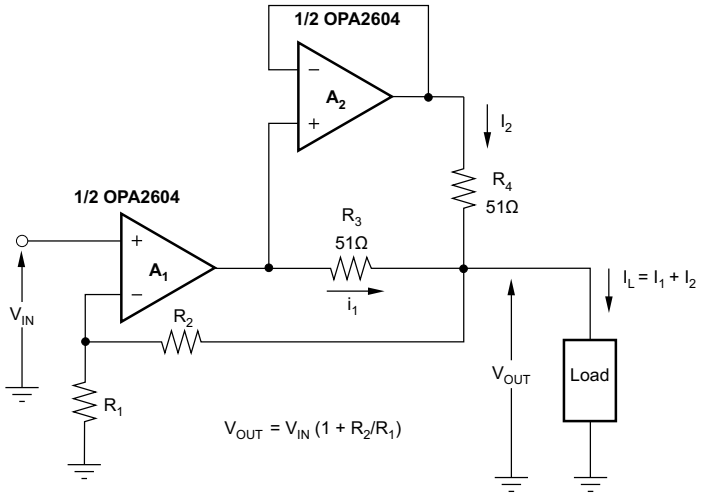


Figure 31. Using the Dual OPA2604 Op Amp to Double the Output Current to a Load

8.2.7.1 Design Requirements

The output current doubler circuit shown in Figure 31 is intended to meet the following design requirements:

- Shares the output current equally between the two amplifiers
- Provides up to twice the maximum current versus using a single amplifier to drive the load
- Wide output swing

Typical Applications (continued)

8.2.8 Three-Pole Low-Pass Filter

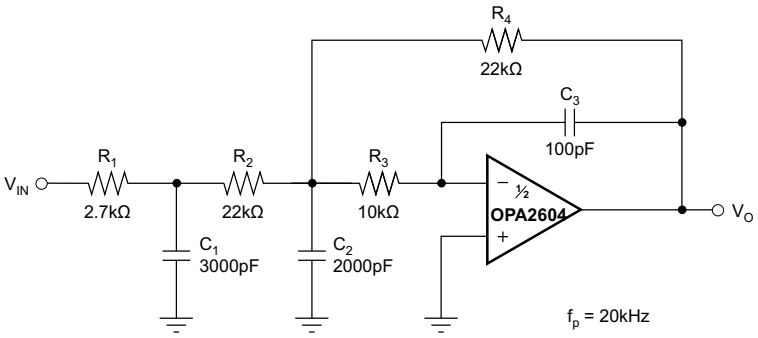


Figure 32. Three-Pole Low-Pass Filter

8.2.8.1 Design Requirements

The low-pass filter shown in Figure 32 is intended to meet the following design requirements:

- Third-order low pass filter response
- 20-kHz cutoff frequency
- Inverting transfer function

9 Power Supply Recommendations

The OPA2604 is unity-gain stable, making it easy to use in a wide range of circuitry. Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins. In most cases, 1-µF tantalum capacitors are adequate.

The OPA2604 is specified for operation from ±4.5 V to ±24 V. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

10 Layout

10.1 Layout Guidelines

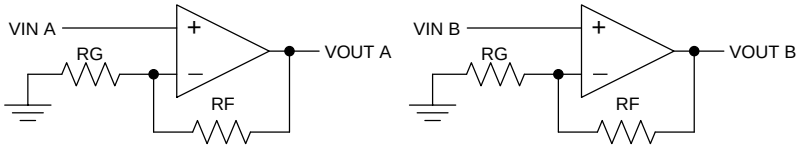
For best operational performance of the device, use good printed-circuit-board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*, SLOA089.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 33, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.1.1 Output Current Limit

Output current is limited by internal circuitry to approximately ±40 mA at 25°C. The limit current decreases with increasing temperature as shown in *Typical Characteristics*.

10.2 Layout Example



(Schematic Representation)

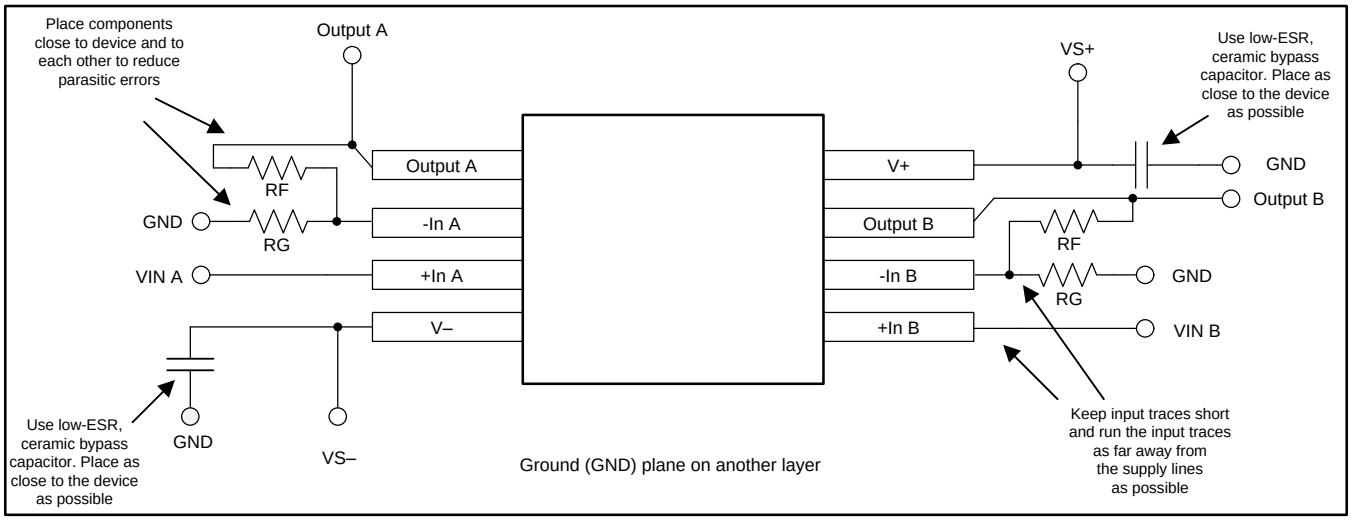


Figure 33. Operational Amplifier Board Layout for Noninverting Configuration

10.3 Power Dissipation

The OPA2604 is capable of driving 600-Ω loads with power supply voltages up to ±24 V. Internal power dissipation is increased when operating at high power supply voltage. Figure 20 shows quiescent dissipation (no signal or no load) as well as dissipation with a worst-case continuous sine wave. Continuous high-level music signals typically produce dissipation significantly less than worst-case sine waves.

The copper leadframe construction used in the OPA2604 improves heat dissipation compared to conventional plastic packages. To achieve best heat dissipation, solder the device directly to the circuit board and use wide circuit board traces.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional DC, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners. Available as a web based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multi-stage active filter solutions within minutes.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.1.2 TI Precision Designs

The OPA2604 is featured in several TI Precision Designs, available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Circuit Board Layout Techniques*, SLOA089.
- *Op Amps for Everyone*, SLOD006.
- *Compensate Transimpedance Amplifiers Intuitively*, SBOA055.
- *Noise Analysis for High Speed Op Amps*, SBOA066.
- *Double the Output Current to a Load With the Dual OPA2604 Audio Op Amp*, SBOA031.
- *Op Amp Performance Analysis*, SBOA054.
- *Single-Supply Operation of Operational Amplifiers*, SBOA059.
- *Tuning in Amplifiers*, SBOA067.
- *Shelf-Life Evaluation of Lead-Free Component Finishes*, SZZA046.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

TINA-TI, E2E are trademarks of Texas Instruments.
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All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2604AP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2604AP	Samples
OPA2604APG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2604AP	Samples
OPA2604AU	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2604AU	Samples
OPA2604AU/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2604AU	Samples
OPA2604AU/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2604AU	Samples
OPA2604AUE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2604AU	Samples
OPA2604AUG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2604AU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

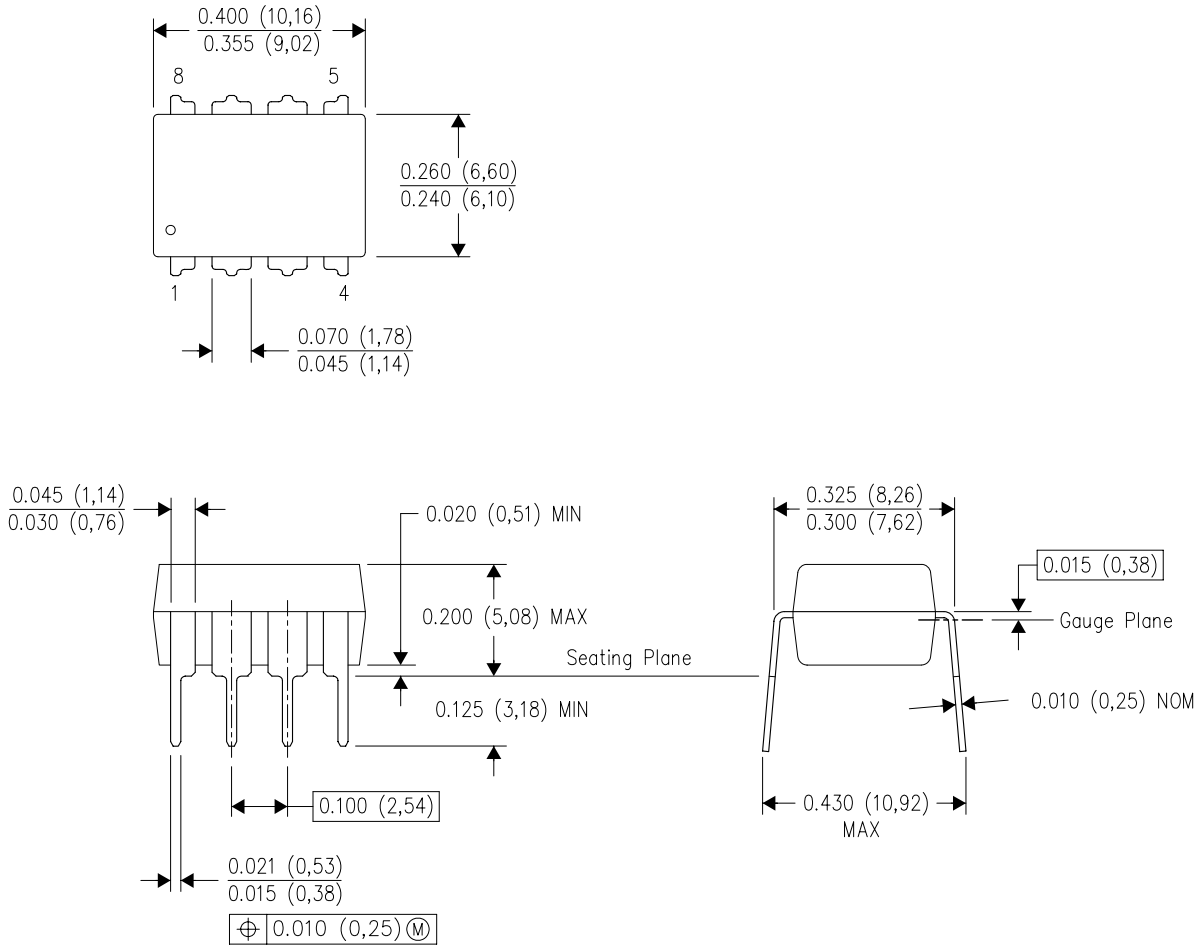
OTHER QUALIFIED VERSIONS OF OPA2604 :

- Automotive: OPA2604-Q1

NOTE: Qualified Version Definitions:

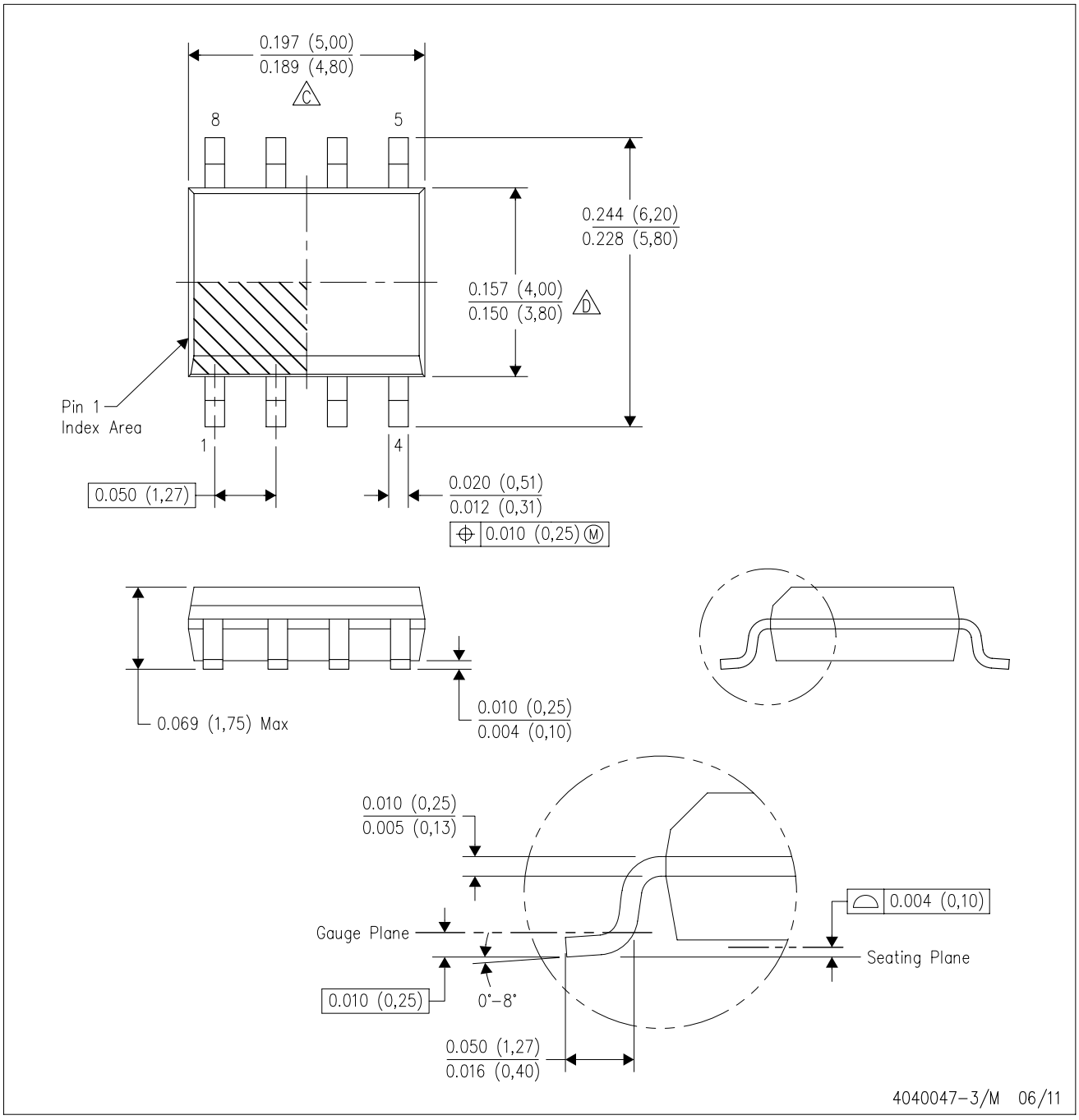
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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